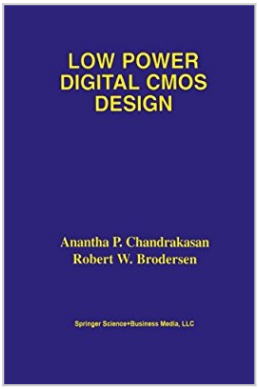

Low Power Digital CMOS Design

By Anantha P. Chandrakasan, Robert W. Brodersen

Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen

Power consumption has become a major design consideration for battery-operated, portable systems as well as high-performance, desktop systems. Strict limitations on power dissipation must be met by the designer while still meeting ever higher computational requirements. A comprehensive approach is thus required at all levels of system design, ranging from algorithms and architectures to the logic styles and the underlying technology.
Potentially one of the most important techniques involves combining architecture optimization with voltage scaling, allowing a trade-off between silicon area and low-power operation. Architectural optimization enables supply voltages of the order of 1 V using standard CMOS technology. Several techniques can also be used to minimize the switched capacitance, including representation, optimizing signal correlations, minimizing spurious transitions, optimizing sequencing of operations, activity-driven power down, etc. The high- efficiency of DC-DC converter circuitry required for efficient, low-voltage and low-current level operation is described by Stratakos, Sullivan and Sanders. The application of various low-power techniques to a chip set for multimedia applications shows that orders-of-magnitude reduction in power consumption is possible.
The book also features an analysis by Professor Meindl of the fundamental limits of power consumption achievable at all levels of the design hierarchy. Svensson, of ISI, describes emerging adiabatic switching techniques that can break the CV^2f barrier and reduce the energy per computation at a fixed voltage. Srivastava, of AT&T, presents the application of aggressive shut-down techniques to microprocessor applications.

Low Power Digital CMOS Design

By Anantha P. Chandrakasan, Robert W. Brodersen

Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen

Power consumption has become a major design consideration for battery-operated, portable systems as well as high-performance, desktop systems. Strict limitations on power dissipation must be met by the designer while still meeting ever higher computational requirements. A comprehensive approach is thus required at all levels of system design, ranging from algorithms and architectures to the logic styles and the underlying technology.
Potentially one of the most important techniques involves combining architecture optimization with voltage scaling, allowing a trade-off between silicon area and low-power operation. Architectural optimization enables supply voltages of the order of 1 V using standard CMOS technology. Several techniques can also be used to minimize the switched capacitance, including representation, optimizing signal correlations, minimizing spurious transitions, optimizing sequencing of operations, activity-driven power down, etc. The high- efficiency of DC-DC converter circuitry required for efficient, low-voltage and low-current level operation is described by Stratakos, Sullivan and Sanders. The application of various low-power techniques to a chip set for multimedia applications shows that orders-of-magnitude reduction in power consumption is possible.
The book also features an analysis by Professor Meindl of the fundamental limits of power consumption achievable at all levels of the design hierarchy. Svensson, of ISI, describes emerging adiabatic switching techniques that can break the CV^2f barrier and reduce the energy per computation at a fixed voltage. Srivastava, of AT&T, presents the application of aggressive shut-down techniques to microprocessor applications.

Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen Bibliography

- Published on: 1995-06-30
- Released on: 1995-06-30
- Original language: English
- Number of items: 1
- Dimensions: 9.25" h x .96" w x 6.10" l, 1.30 pounds
- Binding: Paperback
- 409 pages

Editorial Review

Users Review

From reader reviews:

Deborah Oneal:

Inside other case, little men and women like to read book Low Power Digital CMOS Design. You can choose the best book if you want reading a book. Providing we know about how is important any book Low Power Digital CMOS Design. You can add knowledge and of course you can around the world by way of a book. Absolutely right, because from book you can realize everything! From your country until finally foreign or abroad you may be known. About simple issue until wonderful thing you may know that. In this era, we could open a book or even searching by internet gadget. It is called e-book. You can use it when you feel bored to go to the library. Let's study.

Santa McNabb:

Are you kind of occupied person, only have 10 as well as 15 minute in your day to upgrading your mind expertise or thinking skill actually analytical thinking? Then you are experiencing problem with the book as compared to can satisfy your limited time to read it because all this time you only find guide that need more time to be examine. Low Power Digital CMOS Design can be your answer as it can be read by an individual who have those short free time problems.

Michael Dennison:

The book untitled Low Power Digital CMOS Design contain a lot of information on the idea. The writer explains your girlfriend idea with easy way. The language is very simple to implement all the people, so do definitely not worry, you can easy to read the item. The book was authored by famous author. The author gives you in the new age of literary works. You can actually read this book because you can continue reading your smart phone, or model, so you can read the book with anywhere and anytime. If you want to buy the e-book, you can wide open their official web-site in addition to order it. Have a nice go through.

Jessica Harris:

Is it you who having spare time then spend it whole day by means of watching television programs or just lying on the bed? Do you need something new? This Low Power Digital CMOS Design can be the solution, oh how comes? It's a book you know. You are and so out of date, spending your free time by reading in this completely new era is common not a geek activity. So what these publications have than the others?

Read Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen for online ebook

Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen Free PDF d0wnl0ad, audio books, books to read, good books to read, cheap books, good books, online books, books online, book reviews epub, read books online, books to read online, online library, greatbooks to read, PDF best books to read, top books to read Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen books to read online.

Online Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen ebook PDF download

Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen Doc

Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen Mobipocket

Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen EPub

1HDZU34Y0EF: Low Power Digital CMOS Design By Anantha P. Chandrakasan, Robert W. Brodersen